

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claim in the application.

- 1) (currently amended) A phase locked loop circuit, comprising:
 - a phase-frequency detector to provide a phase difference signal in response to an input signal and a feedback signal;
 - a charge-pump, coupled to the phase-frequency detector, to provide a first voltage in response to the phase difference signal;
 - a filter, coupled to the charge-pump, to provide a second voltage in response to the first voltage;
 - a first voltage-controlled oscillator, coupled to the filter, to provide the feedback signal in response to the second voltage; ~~and,~~
 - a second voltage-controlled oscillator, coupled to the filter, to provide the feedback signal in response to the second voltage; and,
 - a multiplexer, coupled to the first and second voltage-controlled oscillators, to provide the feedback signal in response to the control signal,
 - wherein the charge-pump includes a gain that is adjustable in response to a control signal.
- 2) (cancelled)
- 3) (cancelled)
- 4) (previously presented) The phase locked loop circuit of claim 1, wherein the gain corresponds to a current that is adjustable.
- 5) (previously presented) A phase locked loop circuit, comprising:
 - a phase-frequency detector to provide a phase difference signal in response to an input signal and a feedback signal;
 - a charge-pump, coupled to the phase-frequency detector, to provide a first voltage in response to the phase difference signal;

a filter, coupled to the charge-pump, to provide a second voltage in response to the first voltage;

a first voltage-controlled oscillator, coupled to the filter, to provide the feedback signal in response to the second voltage; and,

a second voltage-controlled oscillator, coupled to the filter, to provide the feedback signal in response to the second voltage;

wherein the charge-pump includes a gain that is adjustable in response to a control signal,

wherein the filter includes a resistor having a resistance that is adjustable in response to the control signal.

- 6) (previously presented) The phase locked loop circuit of claim 1, wherein the filter includes a resistor having a resistance that is adjustable in response to the control signal.
- 7) (previously presented) The phase locked loop circuit of claim 1, further comprising:
a voltage regulator, coupled to the filter and the first and second voltage-controlled oscillators, to provide the second voltage.
- 8) (previously presented) The phase locked loop circuit of claim 7, wherein the voltage regulator includes an operational amplifier.
- 9) (previously presented) The phase locked loop circuit of claim 1, further comprising:
a phase mixer coupled to the first and second voltage-controlled oscillators.
- 10) (previously presented) The phase locked loop circuit of claim 1, further comprising:
a clock buffer coupled to the first and second voltage-controlled oscillators.
- 11) (previously presented) The phase locked loop circuit of claim 1, wherein the filter includes a low-pass filter.

- 12) (previously presented) The phase locked loop circuit of claim 1, wherein the phase locked loop circuit is coupled to a serializer circuit and a deserializer circuit.
- 13) (previously presented) The phase locked loop circuit of claim 12, wherein the phase locked loop circuit, the serializer circuit and deserializer circuit are included in a memory device.
- 14) (previously presented) A phase locked loop circuit, comprising:
 - a phase-frequency detector to provide a phase difference signal in response to an input signal and a feedback signal;
 - a charge-pump, coupled to the phase-frequency detector, to provide a first voltage in response to the phase difference signal;
 - a filter, coupled to the charge-pump, to provide a second voltage in response to the first voltage;
 - an amplifier, coupled to the filter, to provide a buffered voltage in response to the second voltage;
 - a multiplexer, coupled to the amplifier, to provide the buffered voltage in response to a control signal;
 - a first voltage-controlled oscillator, coupled to the multiplexer, to provide the feedback signal in response to the buffered voltage; and,
 - a second voltage-controlled oscillator, coupled to the multiplexer, to provide the feedback signal in response to the buffered voltage.
- 15) (previously presented) The phase locked loop circuit of claim 14, wherein the charge-pump includes a gain that is adjustable in response to the control signal.
- 16) (previously presented) The phase locked loop circuit of claim 15, wherein the gain corresponds to a current that is adjustable.
- 17) (previously presented) The phase locked loop circuit of claim 14, wherein the filter includes a resistor having a resistance that is adjustable in response to the control signal.

- 18) (previously presented) The phase locked loop circuit of claim 14, further comprising:
a phase mixer coupled to the first and second voltage-controlled oscillators.
- 19) (previously presented) The phase locked loop circuit of claim 14, further comprising:
a clock buffer coupled to the first and second voltage-controlled oscillators.
- 20) (previously presented) The phase locked loop circuit of claim 14, wherein the filter
includes a low-pass filter.
- 21) (previously presented) The phase locked loop circuit of claim 14, wherein the phase
locked loop circuit is coupled to a serializer circuit and a deserializer circuit.
- 22) (previously presented) The phase locked loop circuit of claim 21, wherein the phase
locked loop circuit, the serializer circuit and deserializer circuit are included in a memory
device.
- 23) (previously presented) A phase locked loop circuit, comprising:
a phase-frequency detector to provide a phase difference signal in response to an
input signal and a feedback signal;
a charge-pump, coupled to the phase-frequency detector, to provide a first voltage
in response to the phase difference signal;
a filter, coupled to the charge-pump, to provide a second voltage in response to
the first voltage;
a first amplifier, coupled to the filter, to provide a first buffered voltage in
response to the second voltage;
a second amplifier, coupled to the filter, to provide a second buffered voltage in
response to the second voltage;
a first voltage-controlled oscillator, coupled to the first amplifier, to provide the
feedback signal in response to the first buffered voltage; and,

a second voltage-controlled oscillator, coupled to the second amplifier, to provide the feedback signal in response to the second buffered voltage.

- 24) (previously presented) The phase locked loop circuit of claim 23, wherein the charge-pump includes a gain that is adjustable in response to a control signal.
- 25) (previously presented) The phase locked loop circuit of claim 24, wherein the gain corresponds to a current that is adjustable.
- 26) (previously presented) The phase locked loop circuit of claim 23, wherein the filter includes a resistor having a resistance that is adjustable in response to a control signal.
- 27) (previously presented) The phase locked loop circuit of claim 23,
wherein the first amplifier is operational in response to a control signal,
wherein the second amplifier is operational in response to the control signal,
wherein the charge-pump includes a gain that is adjustable in response to the control signal,
wherein the filter includes a resistor having a resistance that is adjustable in response to the control signal.
- 28) (previously presented) The phase locked loop circuit of claim 23, further comprising:
a phase mixer coupled to the first and second voltage-controlled oscillators.
- 29) (previously presented) The phase locked loop circuit of claim 23, further comprising:
a clock buffer coupled to the first and second voltage-controlled oscillators.
- 30) (previously presented) The phase locked loop circuit of claim 23, wherein the filter includes a low-pass filter.

- 31) (previously presented) A method, comprising:
obtaining a phase difference signal in response to an input signal and a feedback signal; and,
providing an adjustable frequency range for the feedback signal in response to a first control signal,
wherein the providing includes adjusting a current in a charge-pump,
wherein the providing includes adjusting a resistance in a filter.
- 32) (previously presented) The method of claim 31, wherein a phase locked loop circuit performs the method.
- 33) (cancelled)
- 34) (cancelled)
- 35) (previously presented) The method of claim 31, wherein the providing includes selecting an output of a multiplexer.
- 36) (previously presented) The method of claim 31, wherein the providing includes selecting an operation of an amplifier.
- 37) (previously presented) The method of claim 31, wherein the providing comprises:
providing the first control signal to the charge-pump;
providing a second control signal to a filter; and,
providing a third control signal to a multiplexer.
- 38) (previously presented) A circuit, comprising:
a phase locked loop circuit to provide an output signal in response to a comparison of an input signal and the output signal; and,
means, coupled to the phase locked loop circuit, for adjusting a frequency range of the output signal in response to a control signal,

wherein the means includes adjusting a current in a charge-pump in response to the control signal,

wherein the means includes adjusting a resistance in a filter.